

Verilog Compile, Synthesis & Simulation

Quartus II

- Altera(현재 Intel)의 FPGA를 위한 FPGA 설계 소프트웨어
- 설계 입력: VerilogHDL, VHDL, AHDL, 또는 schematic을 사용
- Quartus II v9 이전
 - 합성결과에 대한 Simulation 기능 포함, ModelSim 사용 가능
 - 새로운 FPGA에 대한 Simulation은 지원하지 않음
 - Cyclone III까지 지원 (DE2, DE2-70)
- Quartus II v10, v11
 - 합성결과에 대한 Simulation은 ModelSim 등 외부 EDA 도구를 사용해야 함.
 - Cyclone IV도 지원 (DE2, DE2-70, **DE2-115** 사용가능)
- Quartus II v12, v13.0
 - 교육용 목적으로 Simulation 지원 → v13.0 사용 권장
- Quartus II v13.1 이후, 현재 Quartus Prime 17.0
 - Cyclone IV이전 FPGA 지원하지 않음 (DE2, DE2-70 사용 불가)



Quartus II를 이용한 설계/구현 과정

■ 설계

- 프로젝트 생성
- 설계 파일(확장자 .v) 작성
- 컴파일
- 시뮬레이션
 - 시뮬레이션 파형 파일(확장자 .vwf)
 - 시뮬레이션
- 구현 준비
 - 핀번호 할당
 - 컴파일
- 프로그래밍
 - FPGA 프로그래밍



프로젝트 생성 및 설계

Main Quartus II display

😋 Quartus II 64-Bit	_		x
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	New		Ctrl+N	
2	Open		Ctrl+O	
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	New Project W	/izard		
1	Open Project.		Ctrl+J	

■ Project 생성: File > New Project Wizard 🕼 Open Project...

	🚳 New Project Wizard	×
Project 이름은 top module이름과 같게 하는 것이 바람직함	Directory, Name, Top-Level Entity [page 1 of 5] What is the working directory for this project? C:\verilog\register 또는 C:\Verilog What is the name of this project? What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file. register Use Existing Project Settings	
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연세대학교	Project용 directory들 별도로 만들지 않으려면 No	
🌄 김규디 강보공신		t

설계 파일 추가

■ 기존의 설계파일이 준비된 경우에 파일을 추가

							Add
File Name	Type L	.ibrary	Design Entry/Synthesis Tool	HDL Version			Add All
							Remove
							Up
							Down
							Properties



FPGA Device 선택

■ Family: Cyclone II / Device: EP2C35F672C6 (DE2) 또는 EP2C70F896C6 (DE2-70)

■ Family: Cyclone IV E / Device: EP4CE115F29C7 (DE2-115)

나중에 지정 가능



Device family -				_	Show in 'Ava	ailab	ole devices' list			
Family: Cyclo	ne II			-	Package:		Any			Ŧ
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Other: n/a other: n/a ilable devices Name 2C/0F6/2C/ 2C70E672C8	Core Voltage	LEs 68416	User I/Os 422 422	Memo 1152000	ry Bits E 300	Emt	bedded multiplier 9-bit elements	PLL 4	16 16	5
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Other: n/a ailable devices Name 2C/0F6/2C/ 2C70F6/2C8 2C70F6/2C8 2C70F8/96C6 2C70F8/96C6	Core Voltage 1. 2V 1. 2V 1. 2V 1. 2V 1. 2V 1. 2V 1. 2V	LEs 68416 68416 68416 68416 68416	User I/Os 422 422 422 622 622	Memor 1152000 1152000 1152000 1152000 1152000	ry Bits E 300 300 300 300 300 300	E mt)))	bedded multiplier 9-bit elements	PLL 4 4 4 4 4 4	(16 16 16 16	5
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EDA Tool 설정

■ 그대로 [Next] 진행

■ 필요한 경우에는 Simulation 도구 설정 – ModelSim-Altera

DA tools:				-
Tool Type	Tool Name	Format(s)		Run Tool Automatically
esign Entry/Synthesis	<none></none>	✓ <none></none>	7	Run this tool automatically to synthesize the current design
Simulation	<none></none>	✓ <none></none>	v	Run gate-level simulation automatically after compilation
ormal Verification	<none></none>	-		
loard-Level	Timing	<none></none>	•	
	Symbol	<none></none>	•	
	Signal Integrity	<none></none>	-	
	Boundary Scan	<none></none>	T	



Project Wizard 완료 - Summary

Vew Project Wizard	
Summary [page 5 of 5]	
When you click Finish, the project will be create	d with the following settings:
Project directory:	D:\verilog\register
Project name:	register
Top-level design entity:	register
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	Cyclone II
Device:	EP2C70F896C6
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 ℃
	A Back Municipal Circle Council
	< Back Next > Finish Cancel



설계 파일 입력

■ 설계파일 입력 🛄

- File > New> Verilog HDL File
- 새 이름으로 저장
 - File > Save As (default 이름은 project이름.v로 저장)

■ 파일 편집







Compilation

Compile: Processing > Start Compilation

	🔶 register.v 🗵	Compilation Report - register	×
	Table of Contents 🛛 🕂 🗗	Flow Summary	
Tasks Image: Flow: Compilation Customize Flow: Compile Design ✓ <th>Table of Contents 4 6 9 Flow Summary Flow Settings Flow Non-Default Global Setting Flow Elapsed Time Flow OS Summary Flow Log Analysis & Synthesis Flow Messages Flow Suppressed Messages Setting Analyzer</th> <th>Flow Status Quartus II 64-Bit Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total logic elements Dedicated logic registers Total registers Total registers Total pins Total virtual pins Total virtual pins Total memory bits Embedded Multiplier 9-bit elements Total PLLs</th> <th>Successful - Tue Oct 31 11:37:55 2017 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Editio register Cyclone IV E EP4CE115F29C7 Final 4 / 114,480 (< 1 %) 0 / 114,480 (< 1 %) 4 11 / 529 (2 %) 0 0 / 3,981,312 (0 %) 0 / 4 (0 %)</th>	Table of Contents 4 6 9 Flow Summary Flow Settings Flow Non-Default Global Setting Flow Elapsed Time Flow OS Summary Flow Log Analysis & Synthesis Flow Messages Flow Suppressed Messages Setting Analyzer	Flow Status Quartus II 64-Bit Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total logic elements Dedicated logic registers Total registers Total registers Total pins Total virtual pins Total virtual pins Total memory bits Embedded Multiplier 9-bit elements Total PLLs	Successful - Tue Oct 31 11:37:55 2017 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Editio register Cyclone IV E EP4CE115F29C7 Final 4 / 114,480 (< 1 %) 0 / 114,480 (< 1 %) 4 11 / 529 (2 %) 0 0 / 3,981,312 (0 %) 0 / 4 (0 %)





Simulation 준비

■ Waveform 파일생성: (확장자 .vwf)

■ File > New > University Program VWF 메뉴 선택 (Vector Waveform File)







Simulation 입출력 신호 삽입

■ Insert Node or Bus (Signal 선택)



Simulation 입력 신호 값 편집

Grid 지정 – 신호 값 변화가 grid에서 이루어짐



Grid Size...

Set End Time...

Snap to Transition

Snap to Grid

Properties...

L Weak Low (L)

Invert

Weak High (H)

Count Value...

Overwrite Clock...

Arbitrary Value...

Random Values...

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<u>X7</u>

>

Ctrl+Alt+L

Ctrl+Alt+H

Ctrl+Alt+I

Ctrl+Alt+V

Ctrl+Alt+K

Ctrl+Alt+B

Ctrl+Alt+R

■ 신호값 입력 [Edit>Value>값종류] 또는 단축아이콘 선택

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Simulation 입력 신호 값 편집 - 값 0, 1

- 1-bit 값 입력
 - 값을 변경할 영역 선택 → 값 지정 (0, 1, X, Z 또는 INV(반대))





Simulation 입력 신호 값 편집 – 임의의 값

■ Vector값 입력

값을 변경할 영역 선택 → 더블클릭 또는 X2 (Arbitrary Value) → 입력

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Simulation 신호 속성 변경

- 입출력 신호 값 radix 변경 (필요한 경우)
 - 신호 선택 → [Edit > Properties] 선택 또는
 빠른 메뉴(오른쪽 버튼)에서 Properties 선택
 - Radix를 지정





Simulation 입력파일 저장

■ VWF 파일 저장

• [File > Save As] 메뉴 선택

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내 PC 《 네트워크	프로젝트명으로 (여기/ (확장자는 자동적으로	서는 register 부여됨)	() 입력
	< 파일 이름(N): Waveform, vwf 파일 형식(T): University Program VWF (★, vwf) ✓ Add file to current project	•	> 저장(S) 취소



Simulation

- Simulation 시작
 - [Simulation > Run Timing Simulation] 메뉴선택
 - Device의 delay를 고려하여 시뮬레이션 **⊳**© .
 - Functional Simulation : delay를 고려하지 않음

■ Simulation 결과

■ 새 창에 read-only 파일로 생성

🔇 Simulation Waveform Editor -	register.sim.vwf (Read-Only)]	– 🗆 X
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	Simul	ation	Help 🖻
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C	R.	Run F	unctional Simulation
	N.O.	Run T	iming Simulation
	7m	Gener	ate ModelSim Testbench and Script

- 핀번호 및 디바이스 지정

Device 지정

- Device 지정:
 - [Assignments > Device] 메뉴 또는 단축아이콘 🐓 선택
 - Project 생성 시에 지정하지 않았거나 변경할 때 사용



Family: Cyclone II Package: Any Devices: All Pin count: Any Target device Image: Any Pin count: Any O duto device selected by the Fitter Specific devices selected in 'Available devices' list Specific devices: HardCopy compatible only Other: n/a Device and Pin Options Device and Pin Options Available devices: 1.2V S0528 294 S94432 172 EP2CS00484C6 1.2V S0528 294 S94432 172 EP2CS00484C6 1.2V S0528 294 S94432 172 EP2CS00484C8 1.2V S0528 294 S94432 172 EP2C	Family: Cyclone II Package: Any Devices: All	Image: Speed cevices: All Package: Any pet devices: All Pin count: Any pet device Speed grade: Any Auto device selected by the Fitter Speed grade: Any Speed for device selected in 'Available devices' list Speed grade: Any Other: n/a Device and Pin Options bible devices: Speed for devices and Pin Options Store 7218 1.2V 50528 294 Speedrof C 1.2V 50528 294 Store 47218 1.2V 50528 294	amily: Cydone II Devices: AI Package: Any Package: Any Pin count: Any Speed grade: Any Name filter: Specific device selected by the Fitter Specific device selected in 'Available devices' list Other: n/a Name Core Voltage LES User I/OS Verice and Pin Options Value devices: Name Core Voltage LES User I/OS Package: Any Packa	amily: Cyclone II Package: Any arget device Auto device selected by the Fitter Specific devices selected in 'Available devices' list Other: n/a Show advanced devices □ HardCopy compatible only Embedded multiplier 9-bit elements Socore Yoltage LEs User I/Os Memory Bits Embedded multiplier 9-bit elements Socore Yoltage LEs User I/Os Memory Bits Embedded multiplier 9-bit elements Socore Yoltage Les User I/Os Memory Bits Embedded multiplier 9-bit elements Socore Yoltage Les User I/Os Spedific 49/432 T2 Socore Yoltage Les User I/Os Memory Bits Embedded multiplier 9-bit elements T2 Socoutasco T2 Socore Yoltage Socore Yoltage User Yoltage Socore Yoltage	Parkage: Any Devices: All 'arget device Pin count: Any O device selected by the Fitter Specific device selected in 'Available devices' list Package: Any O ther: n/a Specific devices HardCopy compatible only Package: Image: Copy compatible only allable devices: Devices and Pin Options Devices and Pin Options Device and Pin Options allable devices: 1.2V 50528 294 594432 172 20250U484C6 1.2V 50528 294 594432 172 20250U484C7 1.2V 50528 294 594432 172 20250U484C8 1.2V 50528 294	Family: Cyclone II Devices: All Target device Pin count: Auto device selected by the Fitter Speed grade: Specific device selected in 'Available devices' list Name filter: Show advanced devices HardCopy compatible only
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Pin번호 지정

■ 핀번호 지정

■ [Assignment > Pin Planner] 메뉴 또는 단축아이콘 💝 선택

디바이스/핀번호 지정 후에는 다시 compile 해야 함



Device Programming

■ Cable 연결 후 [Tools > Programmer] 메뉴 선택









Block Diagram of DE2 board





Toggle Switches

DE2			DE2-70
Signal Name	FPGA Pin No.	Description	FPGA Pin No.
SW0	PIN_N25	Toggle Switch[0]	PIN_AA23
SW1	PIN_N26	Toggle Switch[1]	PIN_AB26
SW2	PIN_P25	Toggle Switch[2]	PIN_AB25
SW3	PIN_AE14	Toggle Switch[3]	PIN_AC27
SW4	PIN_AF14	Toggle Switch[4]	PIN_AC26
SW5	PIN_AD13	Toggle Switch[5]	PIN_AC24
SW6	PIN_AC13	Toggle Switch[6]	PIN_AC23
SW7	PIN_C13	Toggle Switch[7]	PIN_AD25
SW8	PIN_B13	Toggle Switch[8]	PIN_AD24
SW9	PIN_A13	Toggle Switch[9]	PIN_AE27
SW10	PIN_N1	Toggle Switch[10]	PIN_W5
SW11	PIN_P1	Toggle Switch[11]	PIN_V10
SW12	PIN_P2	Toggle Switch[12]	PIN_U9
SW13	PIN_T7	Toggle Switch[13]	PIN_T9
SW14	PIN_U3	Toggle Switch[14]	PIN_L5
SW15	PIN_U4	Toggle Switch[15]	PIN_L4
SW16	PIN_V1	Toggle Switch[16]	PIN_L7
SW17	PIN_V2	Toggle Switch[17]	PIN_L8





Push Buttons & LEDs

	DE2		DE2-70
Signal Name	FPGA Pin No.	Description	FPGA Pin No.
KEY0	PIN_G26	Pushbutton[0]	PIN_T29
KEY1	PIN_N23	Pushbutton[1]	PIN_T28
KEY2	PIN_P23	Pushbutton[2]	PIN_U30
KEY3	PIN_W26	Pushbutton[3]	PIN_U29



Signal Name	FPGA Pin No.	Description	FPGA Pin No.
LEDR0	PIN_AE23	LED Red[0]	PIN_AJ6
LEDR1	PIN_AF23	LED Red[1]	PIN_AK5
LEDR2	PIN_AB21	LED Red[2]	PIN_AJ5
LEDR3	PIN_AC22	LED Red[3]	PIN_AJ4
LEDR4	PIN_AD22	LED Red[4]	PIN_AK3
LEDR5	PIN_AD23	LED Red[5]	PIN_AH4
LEDR6	PIN_AD21	LED Red[6]	PIN_AJ3
LEDR7	PIN_AC21	LED Red[7]	PIN_AJ2
LEDR8	PIN_AA14	LED Red[8]	PIN_AH3
LEDR9	PIN_Y13	LED Red[9]	PIN_AD14





LEDs (계속)							
	DE2		DE2-70				
LEDR10	PIN_AA13	LED Red[10]	PIN_AC13				
LEDR11	PIN_AC14	LED Red[11]	PIN_AB13				
LEDR12	PIN_AD15	LED Red[12]	PIN_AC12				
LEDR13	PIN_AE15	LED Red[13]	PIN_AB12				
LEDR14	PIN_AF13	LED Red[14]	PIN_AC11				
LEDR15	PIN_AE13	LED Red[15]	PIN_AD9				
LEDR16	PIN_AE12	LED Red[16]	PIN_AD8				
LEDR17	PIN_AD12	LED Red[17]	PIN_AJ7				
LEDG0	PIN_AE22	LED Green[0]	PIN_W27				
LEDG1	PIN_AF22	LED Green[1]	PIN_W25				
LEDG2	PIN_W19	LED Green[2]	PIN_W23				
LEDG3	PIN_V18	LED Green[3]	PIN_Y27				
LEDG4	PIN_U18	LED Green[4]	PIN_Y24				
LEDG5	PIN_U17	LED Green[5]	PIN_Y23				
LEDG6	PIN_AA20	LED Green[6]	PIN_AA27				
LEDG7	PIN_Y18	LED Green[7]	PIN_AA24				
LEDG8	PIN_Y12	LED Green[8]	PIN_AC14				



	DE2		
Signal Name	FPGA Pin No.	Description	FPGA Pin No
HEX0 0	PIN_AF10	Seven Segment Digit 0[0]	PIN_AE8
HEX0 1	PIN_AB12	Seven Segment Digit 0[1]	PIN_AF9
HEX0 2	PIN_AC12	Seven Segment Digit 0[2]	PIN_AH9
HEX0 3	PIN_AD11	Seven Segment Digit 0[3]	PIN_AD10
HEX0 4	PIN_AE11	Seven Segment Digit 0[4]	PIN_AF10
HEX0 5	PIN_V14	Seven Segment Digit 0[5]	PIN_AD11
HEX0 6	PIN_V13	Seven Segment Digit 0[6]	PIN_AD12
HEX10	PIN_V20	Seven Segment Digit 1[0]	PIN_AG13
HEX1 1	PIN_V21	Seven Segment Digit 1[1]	PIN_AE16
HEX12	PIN_W21	Seven Segment Digit 1[2]	PIN_AF16
HEX13	PIN_Y22	Seven Segment Digit 1[3]	PIN_AG16
HEX14	PIN_AA24	Seven Segment Digit 1[4]	PIN_AE17
HEX15	PIN_AA23	Seven Segment Digit 1[5]	PIN_AF17
HEX16	PIN_AB24	Seven Segment Digit 1[6]	PIN_AD17
HEX2 0	PIN_AB23	Seven Segment Digit 2[0]	PIN_AE7
HEX2 1	PIN_V22	Seven Segment Digit 2[1]	PIN_AF7
HEX2 2	PIN_AC25	Seven Segment Digit 2[2]	PIN_AH5
HEX2 3	PIN_AC26	Seven Segment Digit 2[3]	PIN_AG4
HEX2 4	PIN_AB26	Seven Segment Digit 2[4]	PIN_AB18
HEX2 5	PIN_AB25	Seven Segment Digit 2[5]	PIN_AB19
HEX2 6	PIN_Y24	Seven Segment Digit 2[6]	PIN_AE19



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HEX0_DP	PIN_AF12
HEX1_DP	PIN_AC17
HEX2_DP	PIN_AC19

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FPGA Pin No.

PIN_E16

PIN_AD15

PIN_D16

PIN_R28

PIN_R3

PIN_R29

Signal Name

CLK_28

CLK_50

CLK_50_2

CLK_50_3

CLK_50_4

EXT_CLOCK

Clock & text LCD module

	DE2	
Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D13	27 MHz clock input
CLOCK_50	PIN_N2	50 MHz clock input
EXT_CLOCK	PIN_P26	External (SMA) clock input

DE2-70

	IGNO	#2882882888888888888888888888888888888
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Signal Name	FPGA Pin No.	Description	FPGA Pin No.
LCD_DATA[0]	PIN_J1	LCD Data[0]	PIN_E1
LCD_DATA[1]	PIN_J2	LCD Data[1]	PIN_E3
LCD_DATA[2]	PIN_H1	LCD Data[2]	PIN_D2
LCD_DATA[3]	PIN_H2	LCD Data[3]	PIN_D3
LCD_DATA[4]	PIN_J4	LCD Data[4]	PIN_C1
LCD_DATA[5]	PIN_J3	LCD Data[5]	PIN_C2
LCD_DATA[6]	PIN_H4	LCD Data[6]	PIN_C3
LCD_DATA[7]	PIN_H3	LCD Data[7]	PIN_B2
LCD_RW	PIN_K4	LCD Read/Write Select, 0 = Write, 1 = Read	PIN_F3
LCD_EN	PIN_K3	LCD Enable	PIN_E2
LCD_RS	PIN_K1	LCD Command/Data Select, 0 = Command, 1 = Data	PIN_F2
LCD_ON	PIN_L4	LCD Power ON/OFF	PIN_F1
LCD BLON	PIN K2	LCD Back Light ON/OFF	PIN G3

