Quartus-II 사용법

Verilog Compile, Synthesis &
Simulation

Quartus II

- Altera사의 FPGA를 위한 FPGA 설계 소프트웨어
- 설계 입력: VerilogHDL, VHDL, AHDL, 또는 schematic을 사용

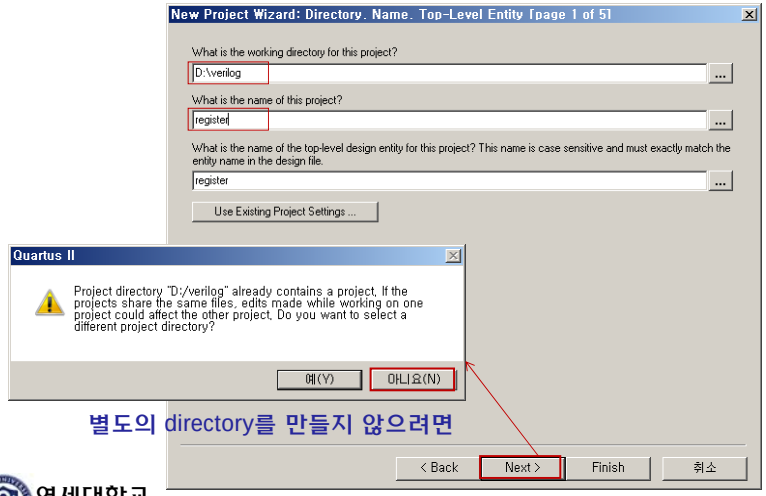
- Quartus II v9 이전
  - 합성결과에 대한 Simulation 기능 포함, ModelSim 사용 가능
  - 새로운 FPGA에 대한 Simulation은 지원하지 않음

- Quartus II v10 이후
  - 합성결과에 대한 Simulation은 ModelSim 등 외부 EDA 도구를 사용해야 함.

Main Quartus II display

설계 시작하기

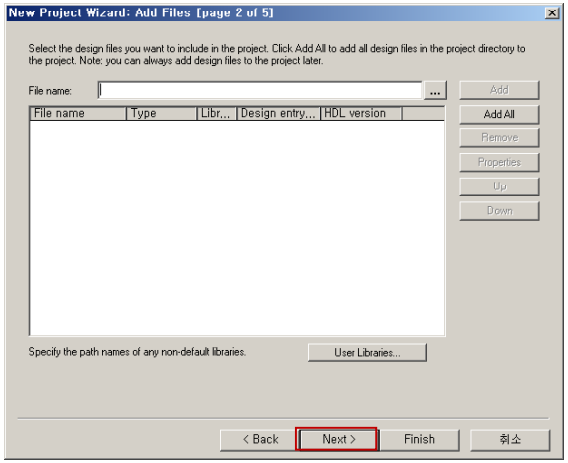
- Project 생성: File > New Project Wizard



별도의 directory를 만들지 않으려면

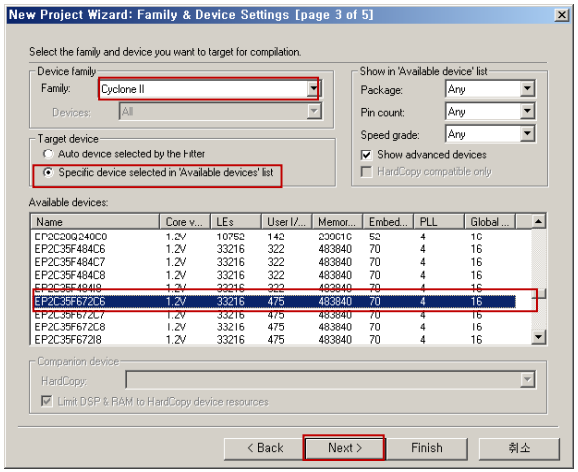
설계 파일 추가

- 기존의 설계파일을 추가 (필요한 경우)



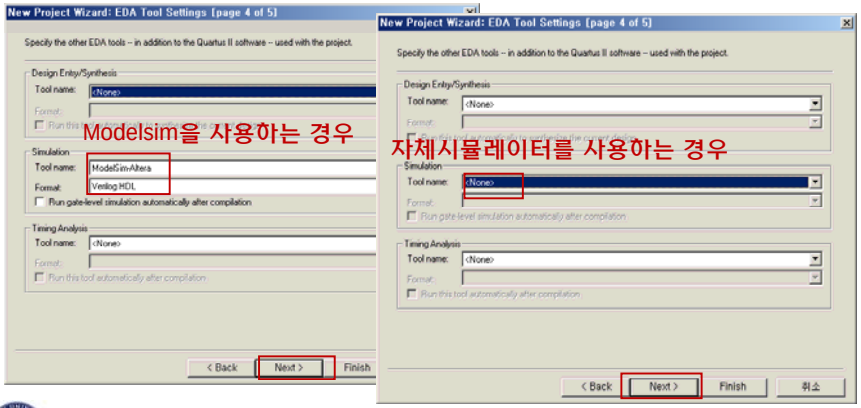
FPGA Device 선택

- Family: Cyclone II
- Device: EP2C35F672C6 (DE2) 또는 EP2C70F896C6 (DE2-70)

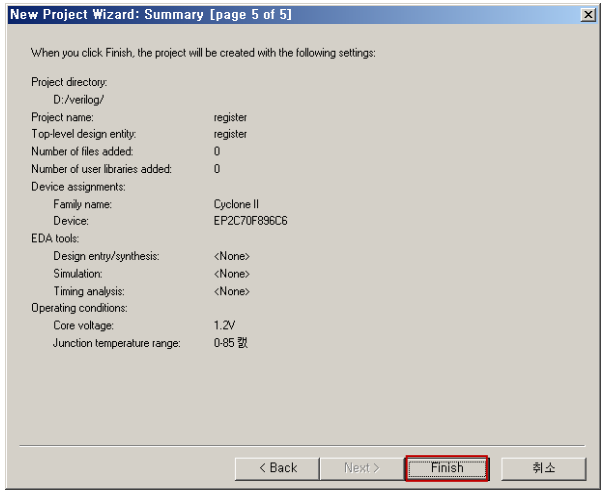


EDA Tool 설정

- Simulation 도구 설정
  - None : 자체 Simulator 사용 또는
  - ModelSim-Altera

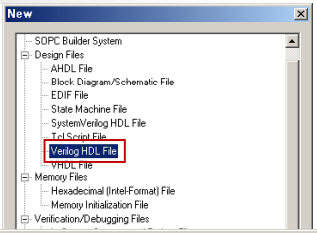


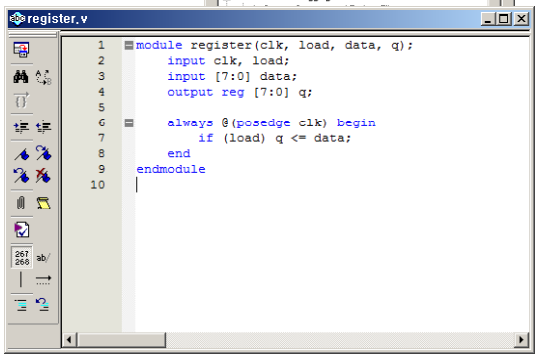
Project Wizard 완료 - Summary



설계 파일 입력

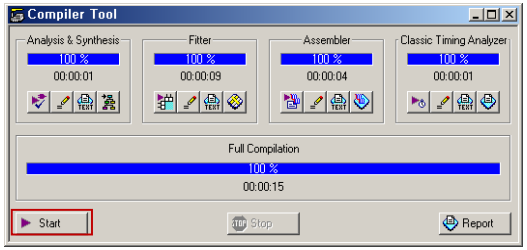
- 설계파일 입력
  - File > New> Verilog HDL File
- 새 이름으로 저장
  - File > Save As
    (default 이름은 project이름.v와 같음)
- 파일 편집





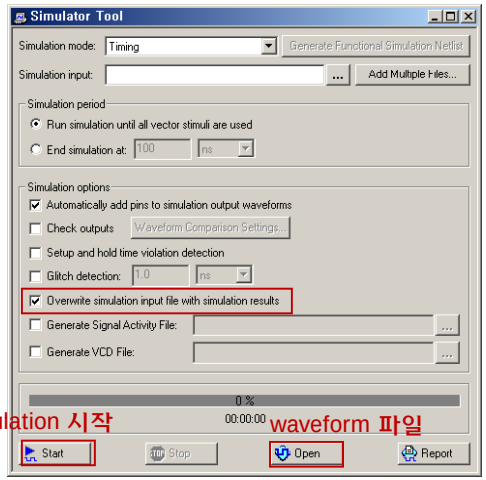
Compilation

- Compile: Processing > Compiler Tool 또는 Start Compilation



Simulation

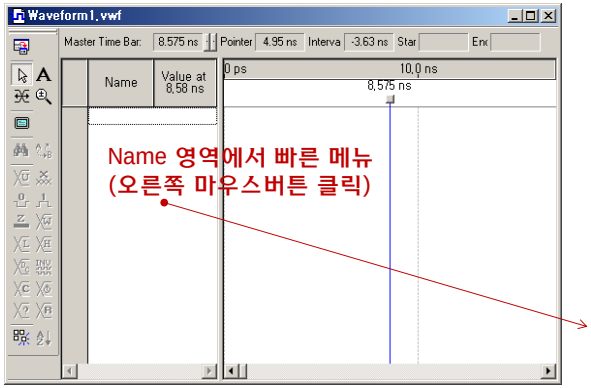
- Simulation: Processing > Simulation Tool
- Waveform 파일 생성: open 선택 → wave form 파일 생성 및 저장
  - 다음 페이지 참조
- Simulation 시작



Simulation 시작 waveform 파일

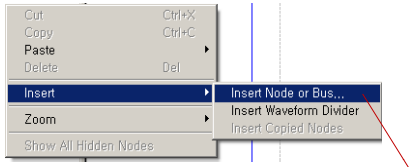
Waveform 파일

- Waveform 파일생성:
  - Simulation Tool에서 Open을 선택하거나
  - File > New > Vector Waveform File 메뉴 선택

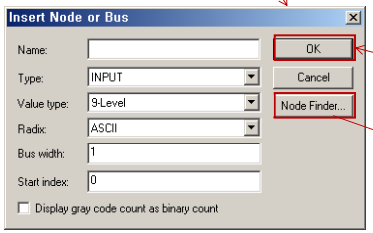


Waveform 파일(2)

- Insert Node or Bus (Signal 선택)
  - Insert Node or Bus (**빠른 메뉴 또는** Edit>Insert> Insert Node or Bus)



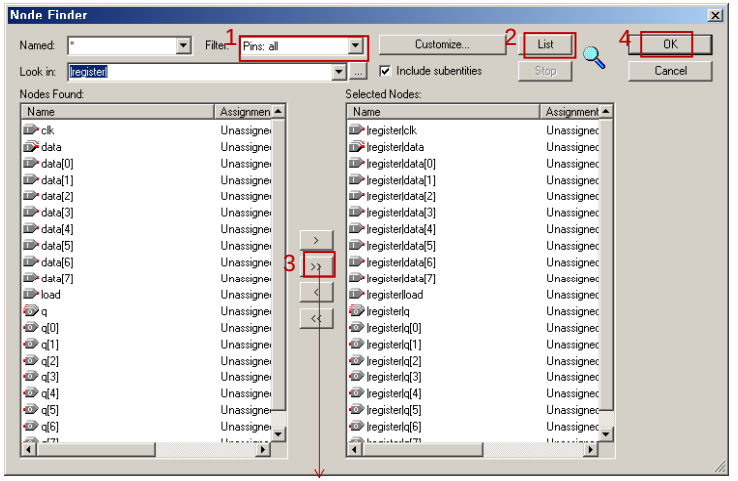
  - Node Finder



Node finder에서
Node 선택 후

Waveform 파일(3)

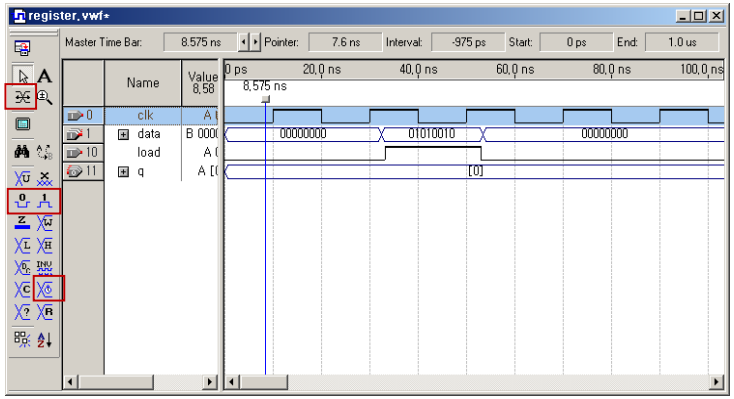
- Node Finder



모든 입출력 신호 선택

Simulation 입력 신호 편집

- 신호 선택 후 입력 값 지정



waveform editing tool

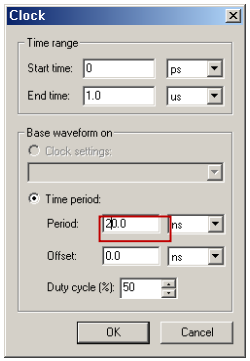
force 0, 1

clock

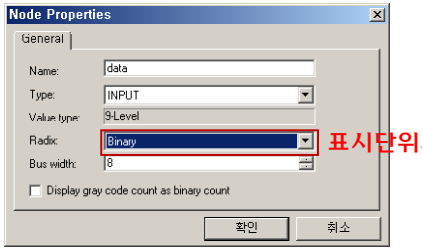
view **메뉴에서** snap to grid**를 해제하면 임의의 시간에 파형변경 가능**

Simulation 입력 신호 편집 (2)

clock **값 지정**

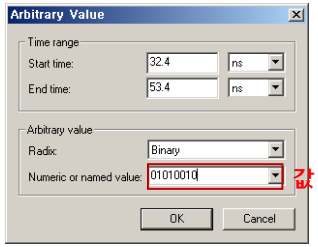


신호이름에서 빠른메뉴 선택 > Node Properties



표시단위지정

화살표 선택 후 파형의 특정 위치에서 더블클릭

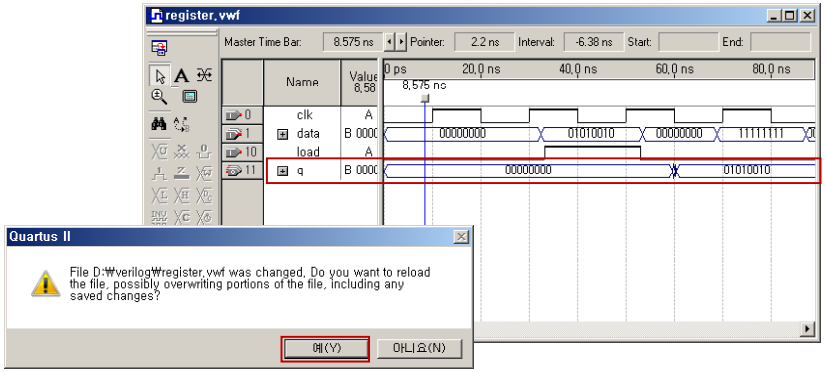


값 지정

- force 0 **또는** force 1**을 사용하여 기본값 지정**
- wave editing tool**에서 파형 값 변경**

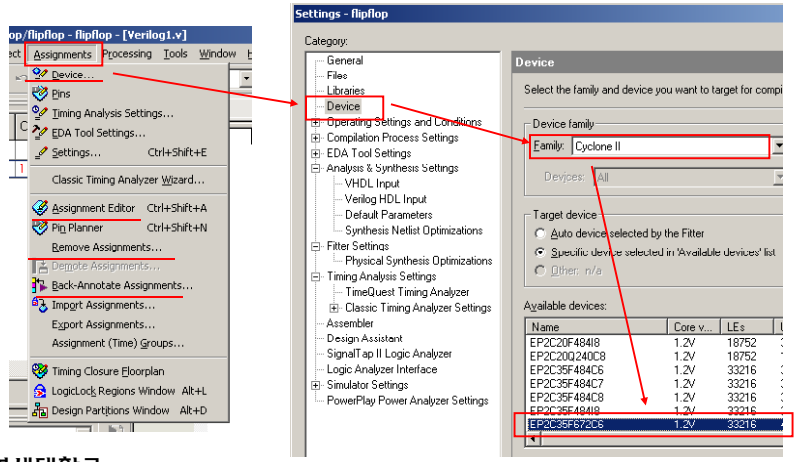
Simulation 시작

- Simulation 시작
  - Simulation Tool에서 Start 버튼 선택하여 Simulation 시작
  - Open을 선택하여 Waveform 파일을 확인 (필요하면 Save change)
    - Simulation 결과가 출력 신호에 반영됨



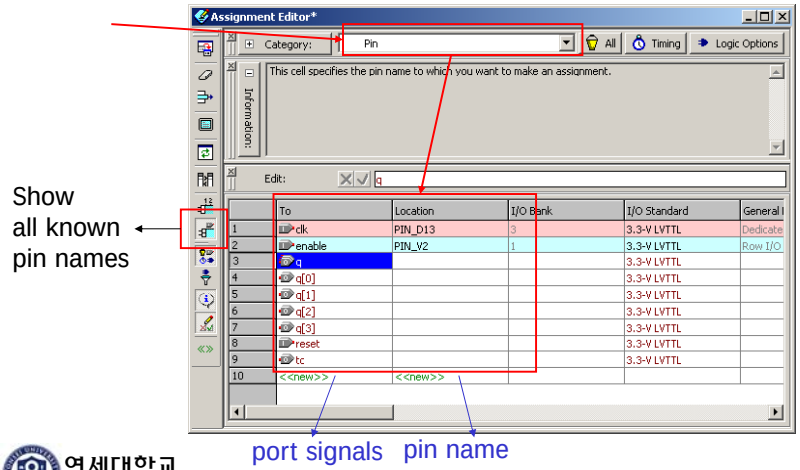
Assignment – Device 지정

- Device: [Assignment > Device]
  - 이미 되어 있으면 생략



Assignment – Pin번호 지정

- Assignment Editor: [Assignment > Assignment Editor]
  또는 Pin: [Assignment > Pin]

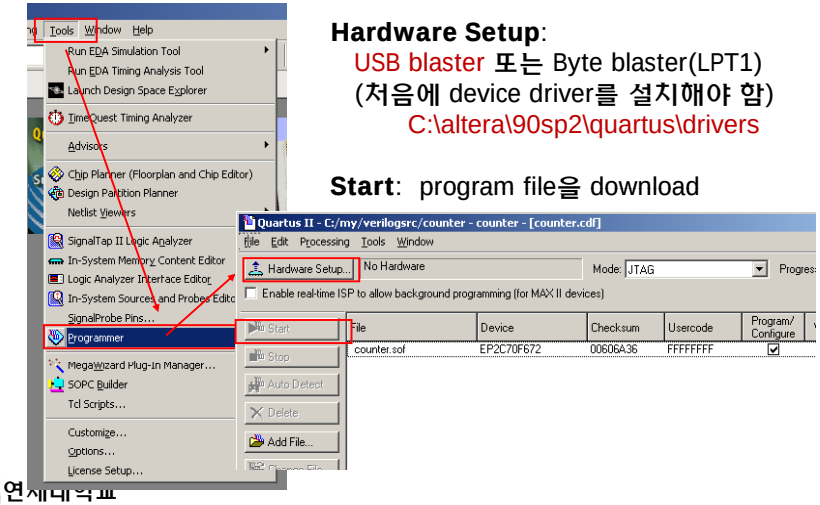


Assignment - 기타

- Back Annotate Assignments
  - Preserve pin, cell, routing, or device assignments
- Remove Assignments
  - Remove existing assignments

Device Programming

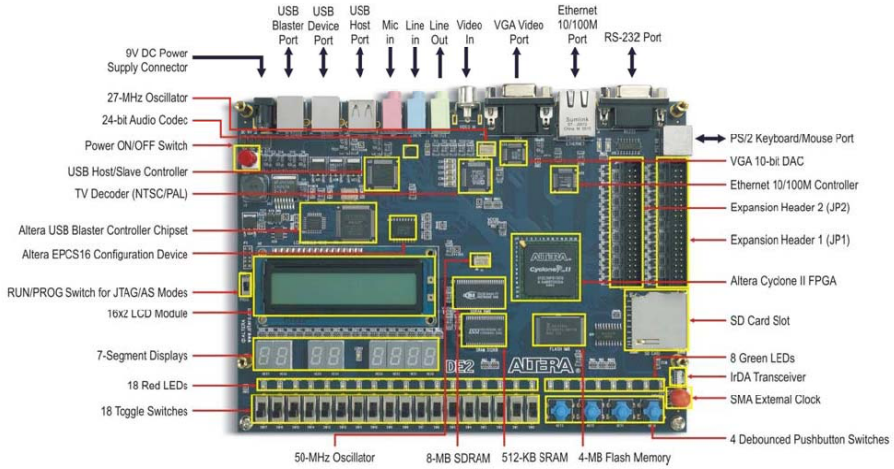
- Cable 연결 후 [Tools > Programmer] 메뉴 선택



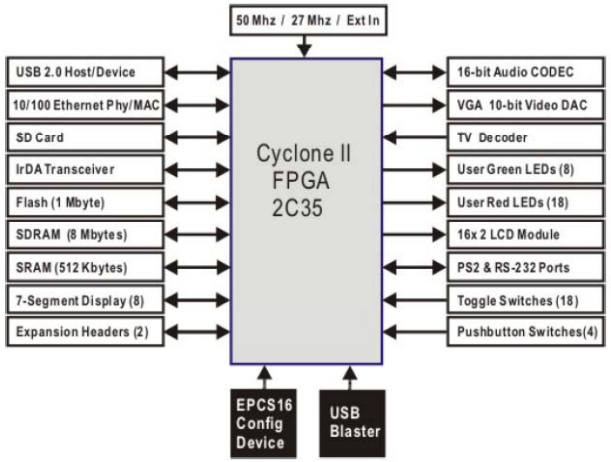
Hardware Setup:
USB blaster 또는 Byte blaster(LPT1)
(처음에 device driver를 설치해야 함)
C:\altera\90sp2\quartus\drivers

Start: program file을 download

Altera DE2 board



Block Diagram of DE2 board



Toggle Switches

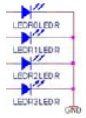
	DE2		DE2-70
Signal Name	FPGA Pin No.	Description	FPGA Pin No.
SW0	PIN_N25	Toggle Switch[0]	PIN_AA23
SW1	PIN_N26	Toggle Switch[1]	PIN_AB26
SW2	PIN_P25	Toggle Switch[2]	PIN_AB25
SW3	PIN_AE14	Toggle Switch[3]	PIN_AC27
SW4	PIN_AF14	Toggle Switch[4]	PIN_AC26
SW5	PIN_AD13	Toggle Switch[5]	PIN_AC24
SW6	PIN_AC13	Toggle Switch[6]	PIN_AC23
SW7	PIN_C13	Toggle Switch[7]	PIN_AD26
SW8	PIN_B13	Toggle Switch[8]	PIN_AD24
SW9	PIN_A13	Toggle Switch[9]	PIN_AE27
SW10	PIN_N1	Toggle Switch[10]	PIN_W5
SW11	PIN_P1	Toggle Switch[11]	PIN_V10
SW12	PIN_P2	Toggle Switch[12]	PIN_U9
SW13	PIN_T7	Toggle Switch[13]	PIN_T9
SW14	PIN_U3	Toggle Switch[14]	PIN_L5
SW15	PIN_U4	Toggle Switch[15]	PIN_L4
SW16	PIN_V1	Toggle Switch[16]	PIN_L7
SW17	PIN_V2	Toggle Switch[17]	PIN_L8

Push Buttons & LEDs

DE2

Signal Name	FPGA Pin No.	Description	DE2-70 FPGA Pin No.
KEY0	PIN_G26	Pushbutton[0]	PIN_T29
KEY1	PIN_N23	Pushbutton[1]	PIN_T26
KEY2	PIN_P23	Pushbutton[2]	PIN_U30
KEY3	PIN_W26	Pushbutton[3]	PIN_U29

Signal Name	FPGA Pin No.	Description	DE2-70 FPGA Pin No.
LEDR0	PIN_AE23	LED Red[0]	PIN_AJ6
LEDR1	PIN_AF23	LED Red[1]	PIN_ AK5
LEDR2	PIN_AB21	LED Red[2]	PIN_AJ5
LEDR3	PIN_AC22	LED Red[3]	PIN_AJ4
LEDR4	PIN_AD22	LED Red[4]	PIN_AK3
LEDR5	PIN_AD23	LED Red[5]	PIN_AH4
LEDR6	PIN_AD21	LED Red[6]	PIN_AJ3
LEDR7	PIN_AC21	LED Red[7]	PIN_AJ2
LEDR8	PIN_AA14	LED Red[8]	PIN_AH3
LEDR9	PIN_Y13	LED Red[9]	PIN_AD14



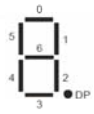
LEDs (계속)

			DE2-70
LEDR10	PIN_AA13	LED Red[10]	PIN_AC13
LEDR11	PIN_AC14	LED Red[11]	PIN_AB13
LEDR12	PIN_AD15	LED Red[12]	PIN_AC12
LEDR13	PIN_AE15	LED Red[13]	PIN_AB12
LEDR14	PIN_AF13	LED Red[14]	PIN_AC11
LEDR15	PIN_AE13	LED Red[15]	PIN_AD9
LEDR16	PIN_AE12	LED Red[16]	PIN_AD8
LEDR17	PIN_AD12	LED Red[17]	PIN_AJ7
LEDG0	PIN_AE22	LED Green[0]	PIN_W27
LEDG1	PIN_AF22	LED Green[1]	PIN_ W25
LEDG2	PIN_W19	LED Green[2]	PIN_ W23
LEDG3	PIN_V18	LED Green[3]	PIN_ Y27
LEDG4	PIN_U18	LED Green[4]	PIN_ Y24
LEDG5	PIN_U17	LED Green[5]	PIN_ Y23
LEDG6	PIN_AA20	LED Green[6]	PIN_ AA27
LEDG7	PIN_Y18	LED Green[7]	PIN_ AA24
LEDG8	PIN_Y12	LED Green[8]	PIN_ AC14

7-segment LED

DE2

Signal Name	FPGA Pin No.	Description	DE2-70 FPGA Pin No.
HEX0 0	PIN_AF10	Seven Segment Digit 0[0]	PIN_AE8
HEX0 1	PIN_AB12	Seven Segment Digit 0[1]	PIN_AF9
HEX0 2	PIN_AC12	Seven Segment Digit 0[2]	PIN_AH9
HEX0 3	PIN_AD11	Seven Segment Digit 0[3]	PIN_AD10
HEX0 4	PIN_AE11	Seven Segment Digit 0[4]	PIN_AF10
HEX0 5	PIN_V14	Seven Segment Digit 0[5]	PIN_AD11
HEX0 6	PIN_V13	Seven Segment Digit 0[6]	PIN_AD12
HEX1 0	PIN_V20	Seven Segment Digit 1[0]	PIN_AG13
HEX1 1	PIN_V21	Seven Segment Digit 1[1]	PIN_AE16
HEX1 2	PIN_W21	Seven Segment Digit 1[2]	PIN_AF16
HEX1 3	PIN_Y22	Seven Segment Digit 1[3]	PIN_AG16
HEX1 4	PIN_AA24	Seven Segment Digit 1[4]	PIN_AE17
HEX1 5	PIN_AA23	Seven Segment Digit 1[5]	PIN_AF17
HEX1 6	PIN_AB24	Seven Segment Digit 1[6]	PIN_AD17
HEX2 0	PIN_AB23	Seven Segment Digit 2[0]	PIN_AE7
HEX2 1	PIN_V22	Seven Segment Digit 2[1]	PIN_AF7
HEX2 2	PIN_AC25	Seven Segment Digit 2[2]	PIN_AH5
HEX2 3	PIN_AC26	Seven Segment Digit 2[3]	PIN_AG4
HEX2 4	PIN_AB26	Seven Segment Digit 2[4]	PIN_AB18
HEX2 5	PIN_AB25	Seven Segment Digit 2[5]	PIN_AB19
HEX2 6	PIN_Y24	Seven Segment Digit 2[6]	PIN_AE19



DE2-70

HEX0_DP	PIN_AF12
HEX1_DP	PIN_ AC17
HEX2_DP	PIN_AC19

Clock & text LCD module

DE2

Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D13	27 MHz clock input
CLOCK_50	PIN_N2	50 MHz clock input
EXT_CLOCK	PIN_P26	External (SMA) clock input

DE2-70

Signal Name	FPGA Pin No.
CLK_28	PIN_E16
CLK_50	PIN_AD15
CLK_50_2	PIN_D16
CLK_50_3	PIN_R28
CLK_50_4	PIN_R3
EXT_CLOCK	PIN_R29

DE2-70

Signal Name	FPGA Pin No.	Description	FPGA Pin No.
LCD_DATA[0]	PIN_J1	LCD Data[0]	PIN_E1
LCD_DATA[1]	PIN_J2	LCD Data[1]	PIN_E3
LCD_DATA[2]	PIN_H1	LCD Data[2]	PIN_D2
LCD_DATA[3]	PIN_H2	LCD Data[3]	PIN_D3
LCD_DATA[4]	PIN_J4	LCD Data[4]	PIN_C1
LCD_DATA[5]	PIN_J3	LCD Data[5]	PIN_C2
LCD_DATA[6]	PIN_H4	LCD Data[6]	PIN_C3
LCD_DATA[7]	PIN_H3	LCD Data[7]	PIN_B2
LCD_RW	PIN_K4	LCD Read/Write Select, 0 = Write, 1 = Read	PIN_F3
LCD_EN	PIN_K3	LCD Enable	PIN_E2
LCD_RS	PIN_K1	LCD Command/Data Select, 0 = Command, 1 = Data	PIN_F2
LCD_ON	PIN_L4	LCD Power ON/OFF	PIN_F1
LCD_BLON	PIN_K2	LCD Back Light ON/OFF	PIN_G3