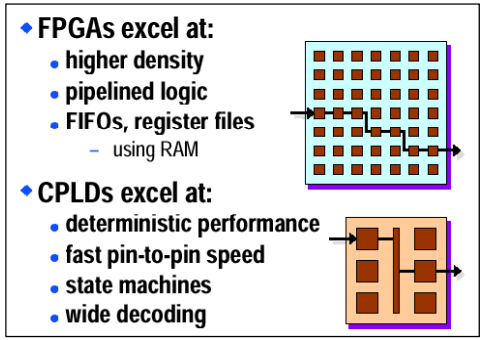
FPGA Device

FPGA와 ASIC

- Field Programmable Gate Array (FPGA)
  - off-the-shelf chips
  - programmable
  - gate array ➔ programmed on logic level
- Application Specific Integrated Circuit (ASIC)
  - chip manufactured for a specific application
  - non-programmable

FPGA와 CPLD

- FPGA (Field Programmable Gate Array)
- CPLD(Complex PLD)



FPGA Markets

- FPGA manufacturers
  - Xilinx (50%) Spartan, Virtex
  - Altera (33%) (Now a part of Intel)
    – Cyclone, Stratix
  - Actel, Atmel, Cypress, Lattice ...
- Markets grown rapidly in 2000's
- Not only competing in their own field
  - Microprocessors
  - Microcontrollers
  - DSPs
  - ASICs

XILINX®

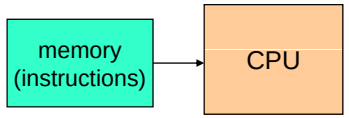
ALTERA®

Programmability of FPGAs

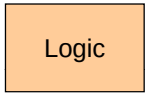
- Device-wide (re)programmability
  - The way in which the device computes can be programmed
  - (cf) In processors, all programmablity is in the program (sequence of instructions); the circuit itself is fixed.
- Where does the programmability come from ?
  - Programmable logic blocks
  - Programmable interface
  - Programmable routing

Programmability Comparison

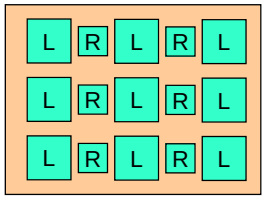
- Processors
  - All programmability is in the program stored in memory



- ASIC
  - No programmability

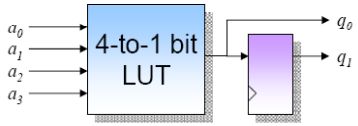


- FPGA
  - device-wide programmability



Programmable Logic Blocks

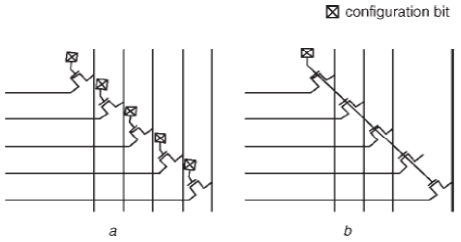
- SRAM-based architecture
- LookUp Table (LUT)-based programmability
  - 4 input bits (address of the SRAM)
  - 1 output bits (output of the SRAM)
- A flip-flop, carry chain logic etc. also attached



LUT stores the truth table of a logic function

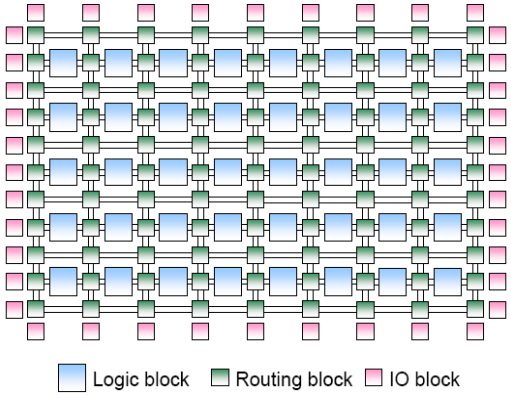
Programmable Routing

- Routings in comercial FPGAs are fine-grained



Fine-grained routing Coarse-grained routing

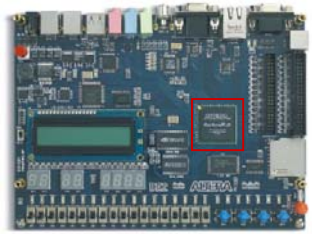
FPGA Architecture



FPGA Lab kit

- HBE Combo
  - Altera ACEX
  - Byte blaster programming (LPT)

- Altera DE2
  - Altera Cyclone II EP2C35 (EP2C35F672C6)
  - USB blaster programming



- Huins FPGA module
  - Altera Cyclone EP1C6 (EP1C6Q240C8)
  - USB blaster programming

ACEX 1K Device Family

Embedded Array Block

Table 1. ACEX™ 1K Device Features

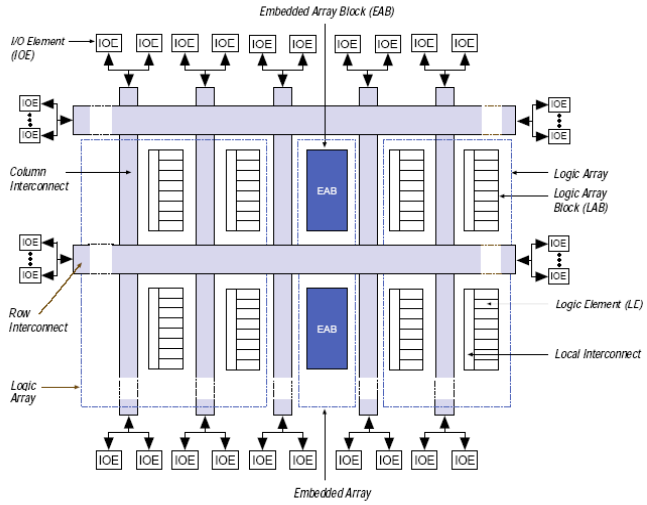
Feature	EP1K10	EP1K30	EP1K50	EP1K100
Typical gates	10,000	30,000	50,000	100,000
Maximum system gates	56,000	119,000	199,000	257,000
Logic elements (LEs)	576	1,728	2,880	4,992
EABs	3	6	10	12
Total RAM bits	12,288	24,576	40,960	49,152
Maximum user I/O pins	136	171	249	333

Table 4. ACEX 1K Device Performance

Application	Resources Used		Performance			
	LEs	EABs	Speed Grade			Units
			-1	-2	-3	
16-bit loadable counter	16	0	285	232	185	MHz
16-bit accumulator	16	0	285	232	185	MHz
16-to-1 multiplexer *(1)*	10	0	3.5	4.5	6.6	ns
16-bit multiplier with 3-stage pipeline *(2)*	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed *(2)*	0	1	278	196	143	MHz
256 × 16 RAM write cycle speed *(2)*	0	1	185	143	111	MHz

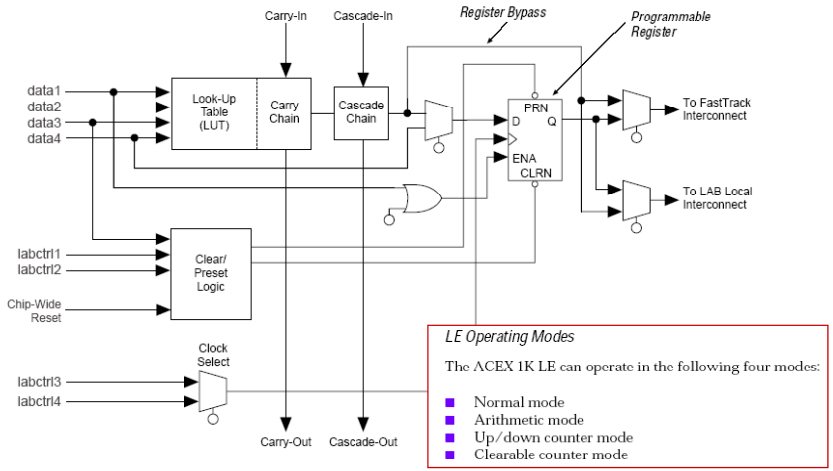
ACEX 1K Block Diagram

Figure 1. ACEX 1K Device Block Diagram



Logical Element

Figure 8. ACEX 1K Logic Element



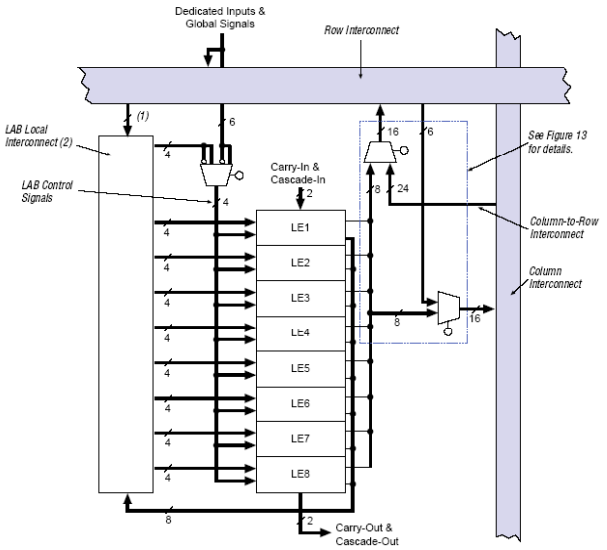
LE Operating Modes

The ACEX 1K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Logical Array Block (LAB)

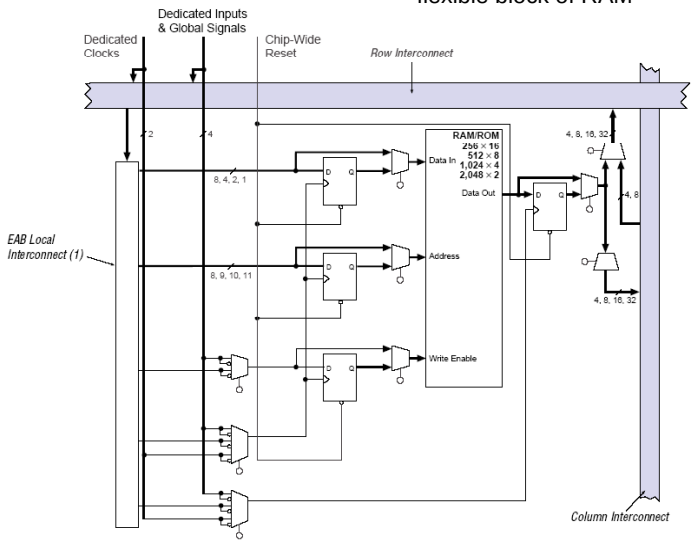
Figure 7. ACEX 1K LAB



Embedded Array Block (EAB)

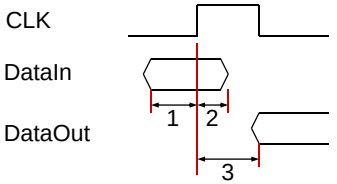
Figure 4. ACEX 1K Device in Single-Port RAM Mode

flexible block of RAM



Timing

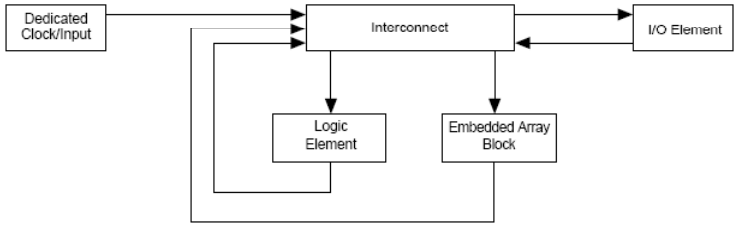
- Setup & Hold Time
  - Clock에 동기되어 동작하는 입력이 Clock의 edge 전/후에 안정되게 입력되어야 하는 최소 시간
- Propagation Delay & Clock-to-Output Delay
  - 회로의 입력의 변화에 대해서 출력이 변화되는 최대 시간
  - Clock에 동기되어 변하는 출력은 Clock edge에서 출력까지의 최대 지연 시간으로 나타냄



1. setup time
2. hold time
3. clock-to-output delay

Timing (계속)

Figure 24. ACEX 1K Device Timing Model

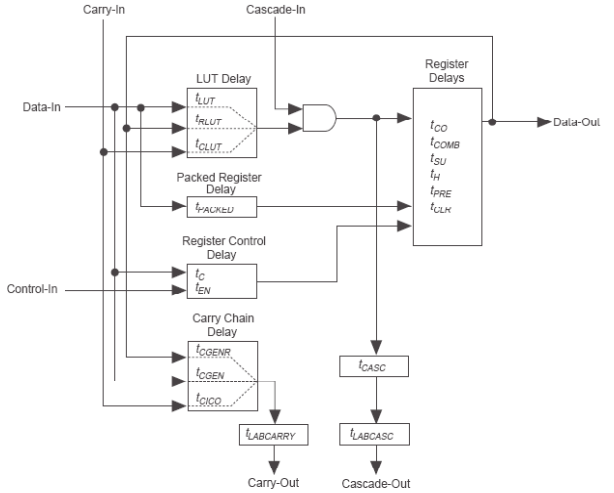


Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay (t_{CO})
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

Timing (계속)

Figure 25. ACEX 1K Device LE Timing Model



Timing (계속)

Table 30. EP1K10 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.5		0.7		0.9	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.7		0.8		1.0		ns
t_{H}	0.9		1.0		1.1		ns

t_{CO} : LE register clock-to-output delay
t_{COMB}: Combinational delay
t_{SU} : LE register setup time
t_{H} : LE register hold time

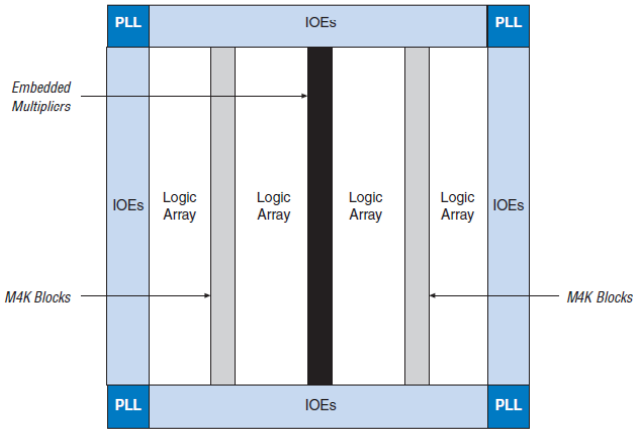
Cyclone II Device Family

Table 1–1. Cyclone II FPGA Family Features

Feature	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	105	129	250
Total RAM bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded multipliers *(1)*	13	18	26	35	86	150
PLLs	2	2	4	4	4	4
Maximum user I/O pins	158	182	315	475	450	622

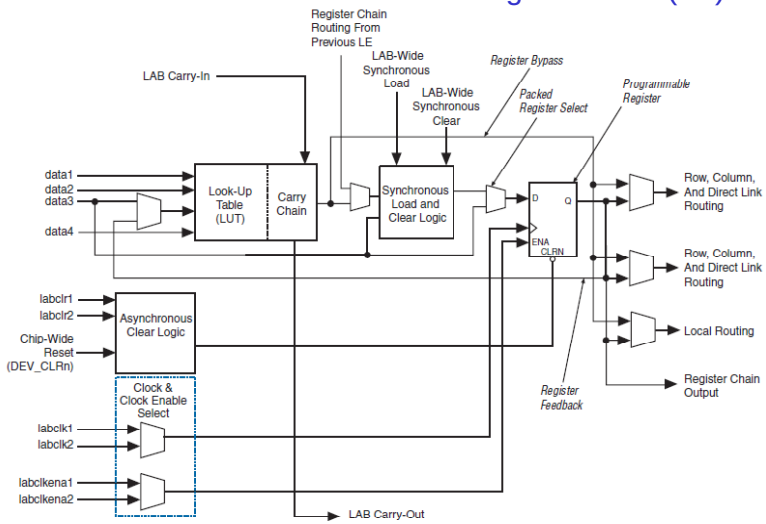
Cyclone II Block Diagram

Figure 2–1. Cyclone II EP2C20 Device Block Diagram



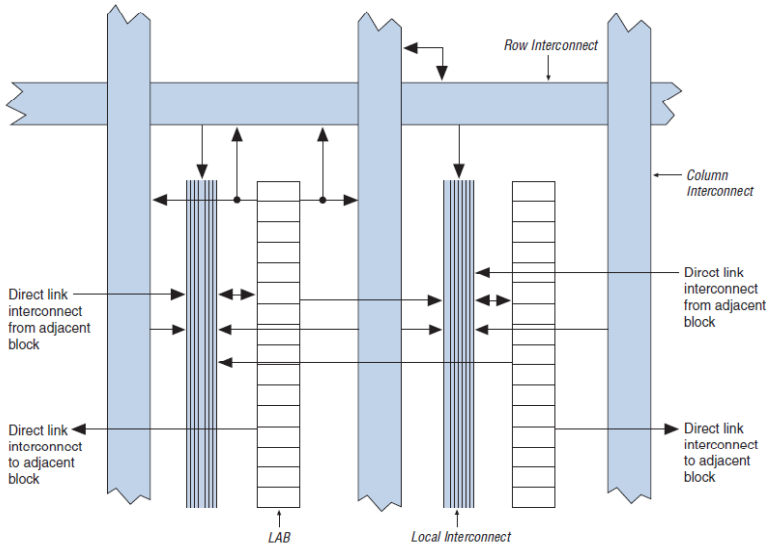
Logic Element(LE)

Figure 2–2. Cyclone II LE



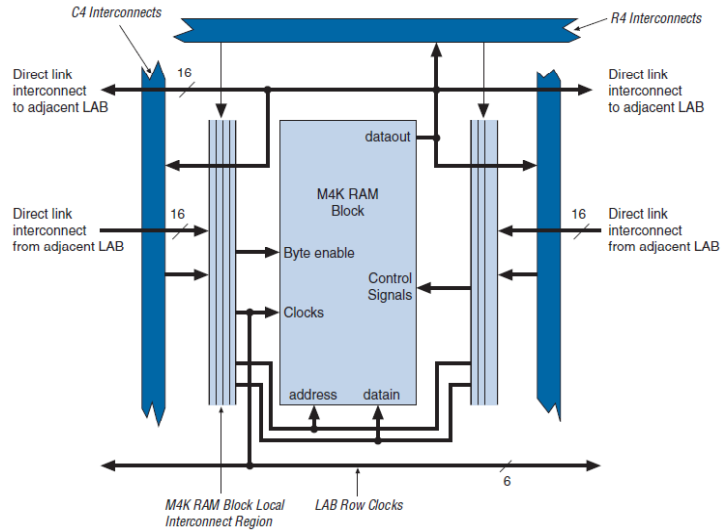
Logic Array Block(LAB)

Figure 2–5. Cyclone II LAB Structure



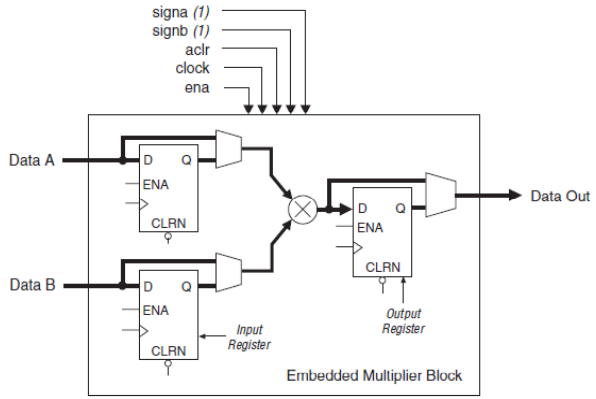
4Kbit RAM block

Figure 2–17. M4K RAM Block LAB Row Interface



Embedded Multiplier Block

Figure 2–18. Multiplier Block Architecture



I/O Element

Figure 2–20. Cyclone II IOE Structure